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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MATTHEWS, COLLEEN ANN	
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2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/876,396	KARIYAZAKI, SYUUICHI	
	Examiner	Art Unit	
	Colleen A. Matthews	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/30/2010 has been entered.

Terminal Disclaimer

The terminal disclaimer filed on 12/30/2010 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of any patent granted on pending Application 12/730,336 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

The delineation of fifth and sixth rows and columns (as in Claim 1) does not have antecedent basis in the Specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites “a first row, a second row, a third row, a first column, a second column and a third column” in lines 9-10 and then goes on to recites “a first row, a first column” line 16; "a second row" line 17; “a second column" lines 17-18; "a fourth row, a fourth column” line 20; “a fifth row” line 21; “a fifth column” line 22. It is unclear if the second recitations of a first row, a second row, a second column, a fourth row, a fourth column, a fifth row, a fifth column were intended to refer to the same rows and columns previously claimed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2 and 4-11 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pat. No. 6,111,756 to Moresco.

Regarding claim 1, Moresco discloses a semiconductor device comprising:

a semiconductor member (Fig 1-2 & 33, element 5) having thereon a plurality of electrode terminals (see Fig 33); and

a mounting member (Fig 1-2, Fig 8, element 20) having a plurality of interconnect pads (within 22; see Figs 2 and 14) electrically and mechanically connected to the respective electrode terminals for mounting the semiconductor member on the mounting member; and

the interconnect pads forming a plurality of I/O cells including signal terminals, a portion of the I/O cells forming a first group (see annotated Fig 14, "+Shape (plus)", for example- first group considered as the outer area of pads labeled "First Group" Please note this is one sample presentation of the interpretation and others that read on the claim language are possible as well.) of I/O cells and another portion of the I/O cells forming a second group (see annotated Fig 14 "+Shape (plus)", for example- second group considered as inner area of pads labeled as "Second Group" Please note this is one sample presentation of the interpretation and others that read on the claim language are possible as well.) of I/O cells on an inner position of the mounting member with respect to the first group of I/O cells,

the first group of I/O cells including a first row, a second row, a third row, a first column, a second column and a third column of interconnect pads (see annotated Figure 14, this example interpretation includes 4 rows and 4 columns, showing

specifically an example of what could be considered as 1st, 2nd, and 3rd rows as well as the 1st, 2nd, and 3rd columns. Please note this is one sample presentation of the interpretation and other interpretations that read on the claim language are possible as well.) disposed to encircle a center of the mounting member, and

the second group of I/O cells including a fourth row, a fifth row, a sixth row, a fourth column, a fifth column and a sixth column of interconnect pads (see annotated Figure 14, this example interpretation has 7 rows and 7 columns, showing specifically an example of what could be considered as 4th, 5th, and 6th rows as well as 4th, 5th, and 6th columns. Please note this is one sample presentation of the interpretation and others that read on the claim language are possible as well) disposed to encircle a center of the mounting member (also col 11 lies 48—col 12 line 40),

the first and second groups of I/O cells being disposed directly under the semiconductor member (see Fig 2), wherein:

the first group of I/O cells arranged in a first row, a first column perpendicular to the first row (see annotated Fig 14), a second row disposed on an inner position relative to the first row, and a second column that is perpendicular to the second row and disposed on an inner position relative to the first column (see annotated Fig 14, arrows indicate second rows and columns inner to first rows and columns)

the second group of I/O cells arranged in a fourth row, a fourth column perpendicular to the fourth row (see annotated Fig 14), a fifth row disposed on an inner position relative to the fourth row, and a fifth column that is perpendicular to the fifth row

and disposed on an inner position relative to the fourth column (see annotated Fig 14, arrows indicate fifth rows and columns inner to fourth rows and columns);

each of the first and second rows and first and second columns of the first group of I/O cells is arranged parallel to at least a portion of an outer periphery of the semiconductor member, and

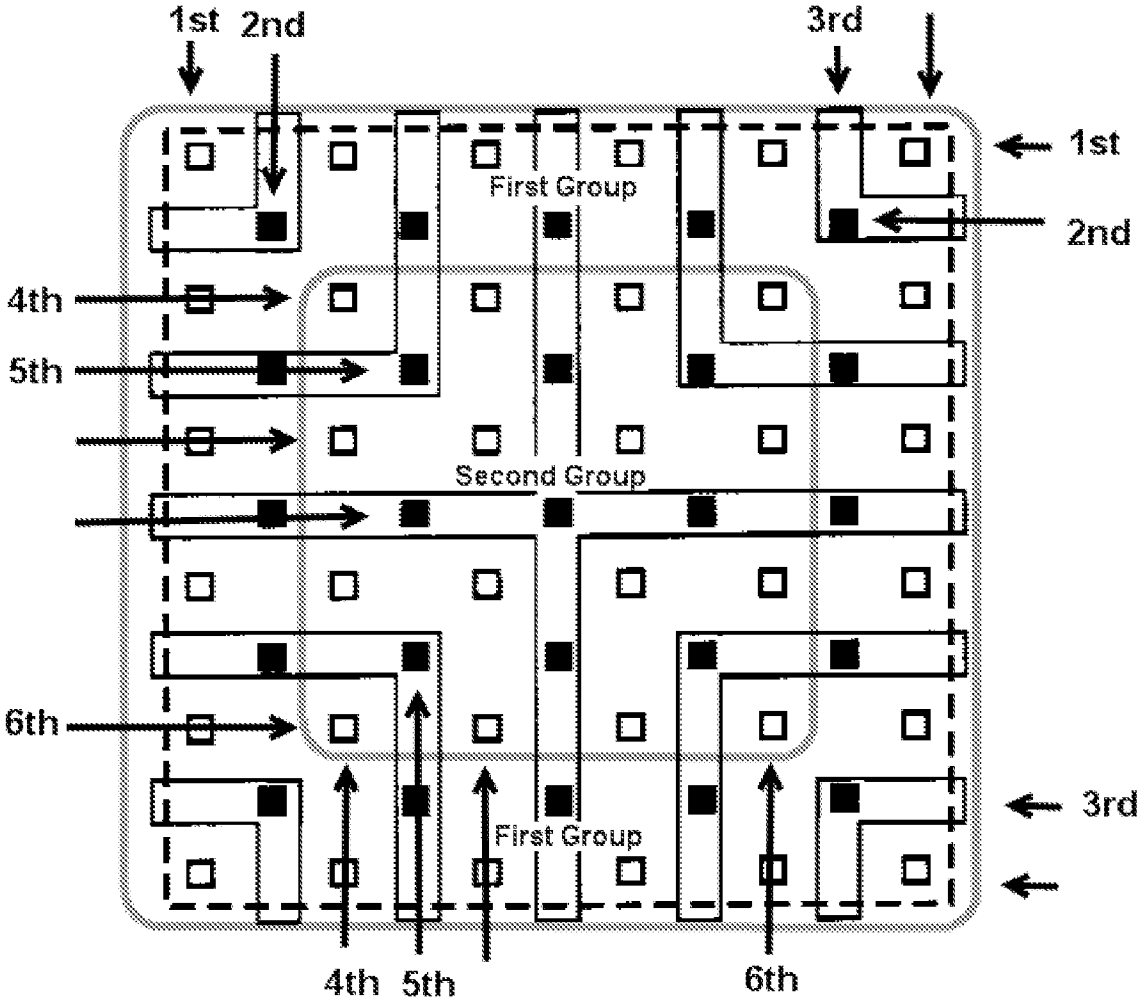
each of the third and fourth rows of the second group of I/O cells is arranged parallel to at least a portion of the outer periphery of the semiconductor member, wherein

the first row, the second row, and the third row of the first group of I/O cells are parallel to one side of the semiconductor member (see annotated Fig 14),

the first column, the second column, and the third column of the first group of I/O cells are parallel to an another side of the semiconductor member(see annotated Fig 14),

the fourth row, the fifth row, mad the sixth row of the second group of I/O cells are parallel to the one side of the semiconductor member (see annotated Fig 14),

and the fourth column, the fifth column, and the sixth column of the second group of I/O cells are parallel to the another side of the semiconductor membe (see annotated Fig 14).



Annotated Figure 14

Regarding claim 2, Moresco discloses a semiconductor device, wherein the semiconductor member is a semiconductor chip (IC chip 5), the electrode terminals are internal electrodes disposed on a bottom surface of the semiconductor chip (shown in Figure 33), and the mounting member is a package substrate used for packaging thereon the semiconductor chip (col 21 lines 21-35).

Regarding claim 4, Moresco discloses a semiconductor device, where the I/O cells only include the signals terminals or terminals for power and ground intermingled among one another (col 5 lines 12-14 ad col 11 lies 43-45).

Regarding claim 5, Moresco discloses a semiconductor device, wherein the I/O cells include peripherals (Fig 1 element 60).

Regarding claim 6, Moresco discloses a semiconductor device, herein an interconnect line (Fig 8, element 42) is electrically connected to each of the interconnect pads and the interconnect lines electrically connected to the interconnect pads of at least one of the I/O cells are formed in a single interconnect layer.

Regarding claim 7, Moresco discloses a semiconductor device, wherein the interconnect pads and the interconnect lines electrically connected to the interconnect pads in the single interconnect layer are formed on the surface of a packaging substrate (see Fig 9).

Regarding claim 8, Moresco discloses a semiconductor device, wherein the interconnect lines connected to the I/O cells located on inner positions extend between the I/O cells located on an outer periphery.

Regarding claim 9, Moresco discloses a semiconductor device, wherein the interconnect pads and the interconnect lines electrically connected to the interconnect pads are formed as a multi-layered interconnect layer in the substrate (see Fig 9).

Regarding claim 10, Moresco discloses a semiconductor device, wherein at least one of the first group (see annotated Fig 14- first group) and the second group (see annotated Fig 14- second group) includes an outer group (see annotated Fig 14-

first group) and inner group (see annotated Fig 14-second group) disposed on the inner position of the mounting member with respect to the outer group (see annotated Fig. 14-first group).

Regarding claim 11, Moresco discloses a semiconductor device, wherein the interconnect lines electrically connected to the interconnect pads corresponding to the first group of I/O cells and interconnect lines electrically connected to the interconnect pads corresponding to the second group of I/0 cells are formed in different interconnect layers (see Fig 9).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moresco as applied to claim 1 above, and further in view of Applicant's Admitted Prior Art of Figure 1 (AAPA).

Regarding claim 3, Moresco discloses a semiconductor device (IC chip 5), wherein the mounting member (chip carrier) is a semiconductor package for mounting the semiconductor chip member on a mounting substrate (see col 2 lines 20-32). Moreseco fails to explicitly disclose the semiconductor package including ball electrodes

disposed on a bottom surface of a packaging substrate, and the mounting substrate forms a specified circuit by mounting the semiconductor package thereon.

AAPA discloses a semiconductor device (103) with the semiconductor package including ball electrodes (124) disposed on a bottom surface of a packaging substrate (102), and the mounting substrate (104) forms a specified circuit by mounting the semiconductor package thereon. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Morseco to include the ball electrodes and configuration of the packaging as in AAPA in order to provide a device capable of connection with other devices in a system.

Response to Arguments

Applicant's arguments filed 12/30/2010 have been fully considered but they are not persuasive.

Applicant argues that it is clear that Moresco teaches outside pads 24and inside pads 22. In response the Examiner notes that Moresco can also be interpreted to show both a first group of I/O cells and a second group of I/O cells as presented in the rejection above, and including all the pertinent rows and columns as claimed.

Further, the Examiner again notes that Applicant's claimed invention provides no clear language that would lead one skilled in the art to consider the distribution of interconnect pads to be solely limited to the interpretation that corresponds to Applicant’s Figures 4 and 7.

One of ordinary skill in the art would be able to construct many alternate interpretations of two groupings of interconnect as presented in the claims, and would not limited solely to the interpretation presented in the rejection above.

Further, the terms "first row", “first column”, “second row”, “second column”, "third row”, “third column”, “fourth row”, “fourth column”, “first group” “second group” do not provide significant definition of the structure of the claimed invention and accordingly will be interpreted broadly in accordance with MPEP 2106, *USPTO personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure. In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997).*

The Examiner notes that the instant application has been rejected again under the previously applied prior art of Moresco. Upon comparison of the Applicant's disclosure and Moresco, there are features, not currently claimed, of Applicant's disclosure that distinguish over the prior art of Moresco. For example, the prior art of Moreseco does not teach the following combined sample limitations drawn from Applicant's specification:

a plurality of I/O cells disposed directly under a semiconductor chip wherein each I/O cell of the plurality of I/O cells consists of an array of 4 x 3 interconnect pads,

wherein the plurality of I/O cells includes at least two outer peripheral I/O cells disposed with a specified interval along a periphery of the semiconductor chip and

wherein the plurality of I/O cells further includes at least one inner I/O cell disposed in an inner section of the semiconductor chip.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen A. Matthews whose telephone number is (571)272-1667. The examiner can normally be reached on Monday - Friday 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Colleen A Matthews/
Examiner, Art Unit 2811